With regard to claim 8, D1 discloses the EDC system as wherein the clock and data recovery module and the electronic dispersion compensation module are embodied in a printed circuit board [D1: pg. 3 para. 0053].

With regard to claim 9, D1 discloses further the EDC system further comprising a receiver that includes the electronic dispersion compensation module [D1: pg. 3 para. 0039].

With regard to claim 10, D1 discloses further the EDC system comprising a transceiver that includes the electronic dispersion compensation module [D1: pg. 1 para. 0006; 12 in Fig. 1; (EDC controller 22) on pg. 1 para. 0009].

With regard to claim 11, D1 discloses an electronic dispersion compensation system [D1: abstract] comprising a clock and data recovery module including a bit error rate module configured to create first data indicating a bit error rate [D1: (SNR and BER) on pg. 1 para. 4; (Data Discriminator 113) on pg. 11 para. 0179; (IS interference) on pg. 11 para. 0189], the clock and data recovery module being configured to send the first data to an electronic dispersion compensation module [D1: (Data Discriminator 113) on pg. 11 para. 0179; (IS interference) on pg. 11 para. 0189], the electronic dispersion compensation module configured to perform a first electronic dispersion compensation solution [D1: FFE 106 in Fig. 2; DFE 114 in Fig. 2; DFE circuit on pg. 2 paras. 0030-0034], the electronic dispersion compensation module including a solution control module configured to receive the first data and to use the first data in determining whether to configure the electronic dispersion compensation module to perform a second electronic dispersion compensation solution [D1: DFE 112 and 114 in Figs. 2 and 8; DFE and FIR on para. 0102; comparator 300 in Fig. 8; DFE 116 on pg. 12 para. 0190].

With regard to claim 12, D1 discloses the EDC system wherein the clock and data recovery module is embodied in a first chip [D1: CDR circuit on pg. 2 para. 0017; (circuits of EDC receiver on “different substrates”) on pg. 7 para. 0120; pg. 3 para. 0053]; and wherein the electronic dispersion compensation module is embodied in a second chip [D1: DFE circuit on pg. 2 para. 0020; (circuits of EDC receiver on “different substrates”) on pg. 7 para. 0120; pg. 3 para. 0053].

With regard to claim 13, D1 discloses the EDC system wherein the clock and data recovery module and the electronic dispersion compensation module are embodied in a printed circuit board [D1: pg. 3 para. 0053].

With regard to claim 14, D1 discloses further the EDC system comprising a receiver that includes the electronic dispersion compensation module [D1: pg. 3 para. 0039].

With regard to claim 15, D1 discloses further the EDC system comprising a transceiver that includes the electronic dispersion compensation module [D1: pg. 1 para. 0006; 12 in Fig. 1; (EDC controller 22) on pg. 1 para. 0009].

With regard to claim 16, D2 discloses an electronic dispersion compensation (EDC) system comprising an electronic dispersion compensation module configured to receive a signal from a backplane [D2: pg. 1 para. 0003] and to apply any of a plurality of electronic dispersion compensation solutions to the signal [D2: 525 in Fig. 5 and pgs. 2-3 para. 0037].

With regard to claim 17, D2 discloses further the EDC system comprising the backplane [D2: pg. 1 para. 0003 and pgs. 2-3 para. 0037].

With regard to claim 18, D2 discloses further the EDC system comprising a receiver that includes the electronic dispersion compensation module [D2: pg. 1 para. 0004, Receiver 520 in Fig. 5].

With regard to claim 19, D2 discloses further the EDC system comprising a transceiver that includes the electronic dispersion compensation module [D2: pg. 1 para. 0004 and pg. 4 para. 0045, XFP 503 in Fig. 5].

With regard to claim 20, D2 discloses further the EDC system comprising a clock and data recovery module including a bit error rate module configured to create first data indicating a bit error rate [D2: 501 in Fig. 5, pg. 1 para. 0003 and pg. 4 para. 0049]; wherein the electronic dispersion compensation module includes a solution control module [D2: 510 in Fig. 5, pg. 3 para. 0039, FFE and DFE on pg. 4 para. 0047] configured to receive the first data and to use the first data in determining whether to configure the electronic dispersion compensation module to switch from applying a first electronic dispersion compensation solution to applying a second electronic dispersion compensation solution [D2: FFE and DFE on pg. 4 para. 0047].

Therefore claims 1-20 are not novel and do not comply with the requirements of Article 33(2) of the PCT.

INVENTIVE STEP (IS)

For the reasons given above the subject matter of claims 1-20 does not meet the requirements of Article 33(3) PCT with regard to inventive step.

