WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International Application No.

PCT/AU2008/XXXXXX

Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims **NONE**	**YES**
	Claims **1-20**	**NO**
Inventive step (IS)	Claims **NONE**	**YES**
	Claims **1-20**	**NO**
Industrial applicability (IA)	Claims **1-20**	**YES**
	Claims **NONE**	**NO**

2. CITATIONS AND EXPLANATIONS:

CITATIONS

D1: US 2004/0258183 A1 (POPESCU et al.) 23 December 2004
D2: US 2006/0067699 A1 (CHANDRASEKHAR et al.) 30 March 2006

NOVELTY (N)

With regard to claim 1, D1 discloses an electronic dispersion compensation (EDC) system [D1: abstract] comprising a clock and data recovery module [D1: CDR in Fig. 2; pg. 2 para. 0018; pg. 4 para. 0075; pg. 5 paras. 0095-0098] including a bit error rate module configured to create first data indicating a bit error rate [D1: (SNR and BER) on pg. 1 para. 4, (AGC and Filter 102) in Fig. 2, (AGC, Filter and SNR) on pgs. 4-5 para. 0092; 104 in Fig. 2]; and an electronic dispersion compensation module configured to perform a first electronic dispersion compensation solution [D1: FFE 106 in Fig. 2; DFE 114 in Fig. 2; DFE circuit on pg. 2 paras. 0030-0034], the electronic dispersion compensation module including a solution control module configured to receive the first data and to use the first data in determining whether to configure the electronic dispersion compensation module to perform a second electronic dispersion compensation solution [D1: DFE 112 and 114 in Figs. 2 and 8; DFE and FIR on para. 0102; comparator 300 in Fig. 8; DFE 116 on pg. 12 para. 0190].

With regard to claim 2, D1 discloses the EDC system wherein the clock and data recovery module is embodied in a first chip [D1: CDR circuit on pg. 2 para. 0017; (circuits of EDC receiver on “different substrates”) on pg. 7 para. 0120; pg. 3 para. 0053]; and wherein the electronic dispersion compensation module is embodied in a second chip [D1: DFE circuit on pg. 2 para. 0020; (circuits of EDC receiver on “different substrates”) on pg. 7 para. 0120; pg. 3 para. 0053].

With regard to claim 3, D1 discloses the EDC system wherein the clock and data recovery module and the electronic dispersion compensation module are embodied in a printed circuit board [D1: pg. 3 para. 0053].

With regard to claim 4, D1 discloses further the EDC system comprising a receiver that includes the electronic dispersion compensation module [D1: pg. 3 para. 0039].

With regard to claim 5, D1 discloses further the EDC system comprising a transceiver that includes the electronic dispersion compensation module [D1: pg. 1 para. 0006; 12 in Fig. 1; (EDC controller 22) on pg. 1 para. 0009].

With regard to claim 6, D1 discloses an electronic dispersion compensation system [D1: abstract] comprising an electronic dispersion compensation module configured to perform a first electronic dispersion compensation solution [D1: FFE 106 in Fig. 2; DFE 114 in Fig. 2; DFE circuit on pg. 2 paras. 0030-0034], the electronic dispersion compensation module including a solution control module configured to receive first data and to use the first data in determining whether to configure the electronic dispersion compensation module to perform a second electronic dispersion compensation solution [D1: DFE 112 and 114 in Figs. 2 and 8; DFE and FIR on para. 0102; comparator 300 in Fig. 8; DFE 116 on pg. 12 para. 0190], the first data indicating a bit error rate, the first data being created by a bit error rate module of a clock and data recovery module [D1: (SNR and BER) on pg. 1 para. 4; (Data Discriminator 113) on pg. 11 para. 0179; (IS interference) on pg. 11 para. 0189].

With regard to claim 7, D1 discloses the electronic dispersion compensation system wherein the clock and data recovery module is embodied in a first chip [D1: CDR circuit on pg. 2 para. 0017; (circuits of EDC receiver on “different substrates”) on pg. 7 para. 0120; pg. 3 para. 0053]; and wherein the electronic dispersion compensation module is embodied in a second chip [D1: DFE circuit on pg. 2 para. 0020; (circuits of EDC receiver on “different substrates”) on pg. 7 para. 0120; pg. 3 para. 0053].

With regard to claim 8, D1 discloses the EDC system as wherein the clock and data recovery module and the electronic dispersion compensation module are embodied in a printed circuit board [D1: pg. 3 para. 0053].

With regard to claim 9, D1 discloses further the EDC system further comprising a receiver that includes the electronic dispersion compensation module [D1: pg. 3 para. 0039].

With regard to claim 10, D1 discloses further the EDC system comprising a transceiver that includes the electronic dispersion compensation module [D1: pg. 1 para. 0006; 12 in Fig. 1; (EDC controller 22) on pg. 1 para. 0009].

With regard to claim 11, D1 discloses an electronic dispersion compensation system [D1: abstract] comprising a clock and data recovery module including a bit error rate module configured to create first data indicating a bit error rate [D1: (SNR and BER) on pg. 1 para. 4; (Data Discriminator 113) on pg. 11 para. 0179; (IS interference) on pg. 11 para. 0189], the clock and data recovery module being configured to send the first data to an electronic dispersion compensation module [D1: (Data Discriminator 113) on pg. 11 para. 0179; (IS interference) on pg. 11 para. 0189], the electronic dispersion compensation module configured to perform a first electronic dispersion compensation solution [D1: FFE 106 in Fig. 2; DFE 114 in Fig. 2; DFE circuit on pg. 2 paras. 0030-0034], the electronic dispersion compensation module including a solution control module configured to receive the first data and to use the first data in determining whether to configure the electronic dispersion compensation module to perform a second electronic dispersion compensation solution [D1: DFE 112 and 114 in Figs. 2 and 8; DFE and FIR on para. 0102; comparator 300 in Fig. 8; DFE 116 on pg. 12 para. 0190].

With regard to claim 12, D1 discloses the EDC system wherein the clock and data recovery module is embodied in a first chip [D1: CDR circuit on pg. 2 para. 0017; (circuits of EDC receiver on “different substrates”) on pg. 7 para. 0120; pg. 3 para. 0053]; and wherein the electronic dispersion compensation module is embodied in a second chip [D1: DFE circuit on pg. 2 para. 0020; (circuits of EDC receiver on “different substrates”) on pg. 7 para. 0120; pg. 3 para. 0053].

With regard to claim 13, D1 discloses the EDC system wherein the clock and data recovery module and the electronic dispersion compensation module are embodied in a printed circuit board [D1: pg. 3 para. 0053].

With regard to claim 14, D1 discloses further the EDC system comprising a receiver that includes the electronic dispersion compensation module [D1: pg. 3 para. 0039].

With regard to claim 15, D1 discloses further the EDC system comprising a transceiver that includes the electronic dispersion compensation module [D1: pg. 1 para. 0006; 12 in Fig. 1; (EDC controller 22) on pg. 1 para. 0009].

With regard to claim 16, D2 discloses an electronic dispersion compensation (EDC) system comprising an electronic dispersion compensation module configured to receive a signal from a backplane [D2: pg. 1 para. 0003] and to apply any of a plurality of electronic dispersion compensation solutions to the signal [D2: 525 in Fig. 5 and pgs. 2-3 para. 0037].

With regard to claim 17, D2 discloses further the EDC system comprising the backplane [D2: pg. 1 para. 0003 and pgs. 2-3 para. 0037].

With regard to claim 18, D2 discloses further the EDC system comprising a receiver that includes the electronic dispersion compensation module [D2: pg. 1 para. 0004, Receiver 520 in Fig. 5].

With regard to claim 19, D2 discloses further the EDC system comprising a transceiver that includes the electronic dispersion compensation module [D2: pg. 1 para. 0004 and pg. 4 para. 0045, XFP 503 in Fig. 5].

With regard to claim 20, D2 discloses further the EDC system comprising a clock and data recovery module including a bit error rate module configured to create first data indicating a bit error rate [D2: 501 in Fig. 5, pg. 1 para. 0003 and pg. 4 para. 0049]; wherein the electronic dispersion compensation module includes a solution control module [D2: 510 in Fig. 5, pg. 3 para. 0039, FFE and DFE on pg. 4 para. 0047] configured to receive the first data and to use the first data in determining whether to configure the electronic dispersion compensation module to switch from applying a first electronic dispersion compensation solution to applying a second electronic dispersion compensation solution [D2: FFE and DFE on pg. 4 para. 0047].

Therefore claims 1-20 are not novel and do not comply with the requirements of Article 33(2) of the PCT.

INVENTIVE STEP (IS)

For the reasons given above the subject matter of claims 1-20 does not meet the requirements of Article 33(3) PCT with regard to inventive step.

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INDUSTRIAL APPLICABILITY (IA)

The invention defined in the claims is considered to meet the requirements of Industrial Applicability under Article 33(4) of the PCT because it can be made by, or used in, industry.